In the Claims:

1. (Currently Amended) A lateral thin-film Silicon-On-Insulator (SOI) device comprising

a semiconductor substrate,

a buried insulating layer on said substrate, and

a lateral MOS transistor device in an SOI layer on said buried insulating layer and having

a source region of a first type conductivity formed in a body region of a second type conductivity,

a lateral drift region of a second type conductivity adjacent said body region,

a drain region of said first type conductivity and laterally spaced apart from said body region ~~by said lateral drift region~~,

a gate electrode insulated from said body region and drift region by an insulation region,

an insulation layer on and laterally adjacent to the gate electrode, and

a field plate on the insulation layer and separated from the gate electrode and the drain extension region by the insulation layer, the field plate being connected either to said source region or said gate electrode and extending substantially over said lateral drift region, wherein said field plate comprises a first layer of plural metallic regions which are isolated laterally from one another so as to form a linear lateral electric field distribution in the lateral drift region.

2. (Currently Amended) A lateral thin-film Silicon-On-Insulator (SOI) of claim 1 wherein said isolated metallic regions are located in a layer that is vertically above a layer including the gate electrode, and are isolated from one another by a dielectric layer.

3. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 2 wherein said field plate further comprises another layer of plural metallic regions located above said spaces, laterally isolated from one another, and isolated from said metallic regions of said first layer by said dielectric layer.

4. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 3 wherein said dielectric layer is a silicon-rich nitride layer.

5. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 4 further comprises another dielectric layer provided between said field plate and said MOS transistor device.

6. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 1 wherein said lateral drift region is provided with a linearly-graded charge profile.

7. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 6 wherein said linear lateral electric field distribution follows an electric field in said drift region.

8. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 7 wherein said first type conductivity is p-type conductivity, and said second type conductivity is n-type conductivity.

9. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 3 wherein said first type conductivity is p-type conductivity, and said second type conductivity is n-type conductivity.

10. (Original) A lateral thin-film Silicon-On-Insulator (SOI) of claim 1 wherein said first type conductivity is n-type conductivity, and said second type conductivity is p-type conductivity.

11. (Previously presented) A lateral thin-film Silicon-On-Insulator (SOI) of claim 1 wherein a first one of said metallic regions in the field plate is connected to said source region and the remaining ones of said metallic regions are capacitively coupled to the first one of said metallic regions to linearly distribute a voltage at the source region across the field plate.

12. (Previously presented) A lateral thin-film Silicon-On-Insulator (SOI) of claim 1 wherein a first one of said metallic regions in the field plate is connected to said gate electrode and the remaining ones of said metallic regions are capacitively coupled to the first one of said metallic regions to linearly distribute a voltage at the gate electrode across the field plate.

13. (Currently Amended) A lateral thin-film Silicon-On-Insulator (SOI) device comprising

a semiconductor substrate;

a buried insulating layer on the substrate; and

a lateral MOS transistor device in an SOI layer on said buried insulating layer and having

a source region of a first conductivity type formed in a body region of a second conductivity type,

a lateral drift region of the second conductivity type adjacent the body region,

a drain region of the first conductivity type and laterally spaced apart from the body region by the lateral drift region,

a gate electrode insulated from said body region and drift region by an insulation region,

an insulation layer on and laterally adjacent to the gate electrode,

source and drain contact regions in a layer region including the gate electrode and respectively electrically contacting the source and drain regions, the contact regions being laterally separated from the gate electrode by the insulation layer and

a field plate arrangement, on the insulation layer, having a plurality of conductive regions that laterally extend substantially over the lateral drift region and that are insulated from one another by an insulative material, a first one of the conductive regions at a first end of the field plate being connected either to the source region or the gate electrode, the conductive regions linearly distributing a voltage at the first conductive region across the other conductive regions to an opposite end of the field

plate, the distributed voltage ~~drops~~ dropping laterally across the field plate from the first end to the opposite end.

14. (Previously presented) The device of claim 13, wherein the field plate arrangement linearly distributes an electric field across the lateral drift region.

15. (Previously presented) The device of claim 13, wherein the field plate arrangement provides a linearly-graded charge profile to the lateral drift region, the charge profile dropping linearly from a high charge profile below the first end of the field plate arrangement to a low charge profile below the opposite end of the field plate arrangement.

16. (New) The device of claim 1, further including

a source contact region electrically coupled to the source region, having an extension above the gate on the insulation layer, and being separated both laterally and vertically from the gate electrode by the insulation layer, and

a drain contact region electrically coupled to the drain region, having an extension on the insulation layer, and being separated laterally from the gate electrode by the insulation layer,

the field plate extending between the extensions of the source contact region and the drain contact region on the insulation layer.